2.488/2.667 GBPS STS-48/STM-16 SONET/SDH XRT91L80 Transceiver Evaluation Board User Manual

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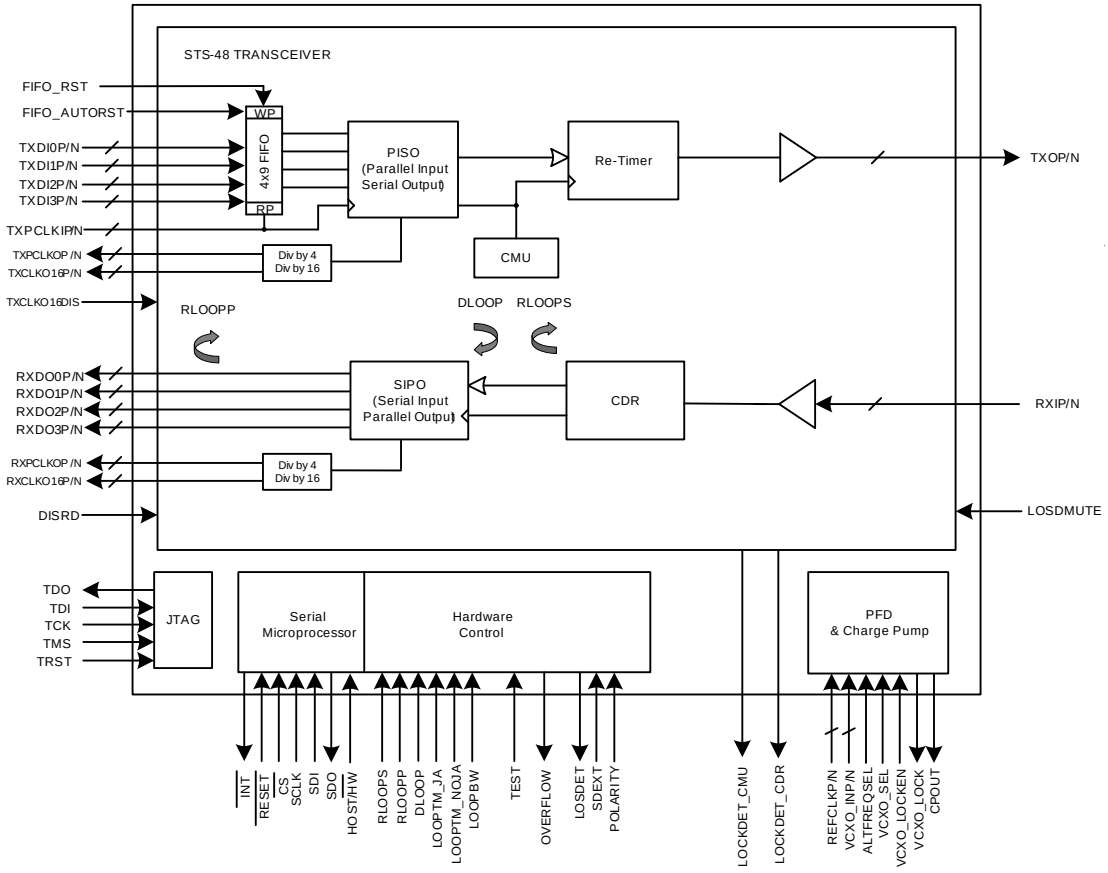
Figure 1.0 XRT91L80 Block Diagram



1.0 OVERVIEW

This is evaluation board manual is intended to help the user become familiarized to operate the XRT91L80 Evaluation Demo Board and run traffic with minimum effort.

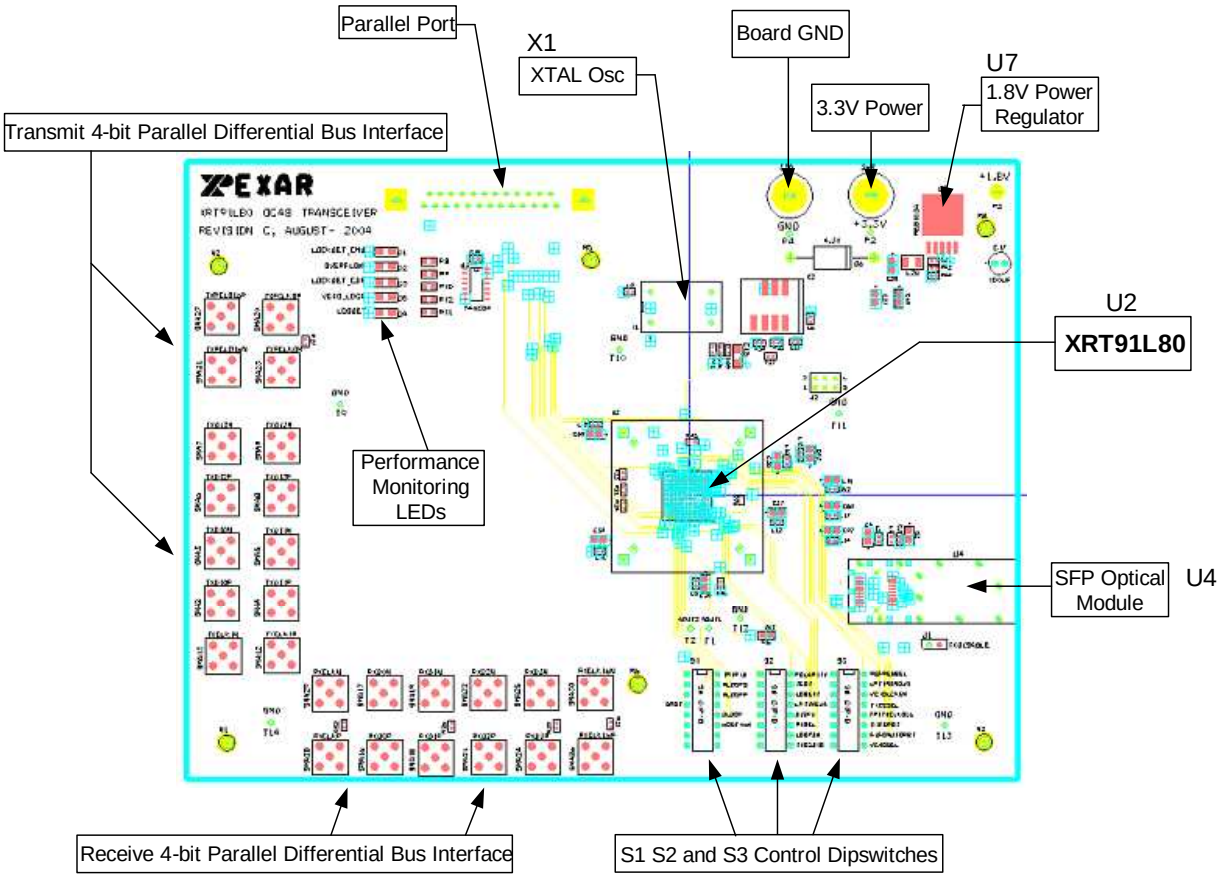
Requirements:

1. XRT91L80 Evaluation Demo board
2. 3.3V Lab power supply and 2 banana leads
3. OC-48/STM-16 generator/analyzer test equipment with optical interface
4. An optional Windows PC with parallel port & parallel cable for HOST mode (may be run in Hardware mode as shipped)
5. XRT91L80 supplied GUI to be installed on the PC (using Win98, 2000, or XP)
6. XRT91L80 data sheet (rev P1.1.0)
7. (optional) A Parallel Bit Error Tester if parallel bus interface testing is desired
8. (optional) 20 high quality SMB coax cables for parallel interface connections

2.0 Evaluation Board Architecture

XRT91L80 Evaluation Board provides a simple and efficient way to quickly evaluation functionality and performance of the XRT91L80 SONET/SDH STS-48/STM-16 Transceiver.

Figure 2.0 XRT91L80 Evaluation Board Revision C



Evaluation board consists of XRT91L80 device (U2) connected to a Small Form Factor Pluggable (SFP) optical module (U4). The XRT91L80 hardware control pins are interfaced to three control dipswitches (S1, S2, and S3). The logical level of the XRT91L80 hardware control pins are either toggled “high” or “low” depending on state or position of switches.

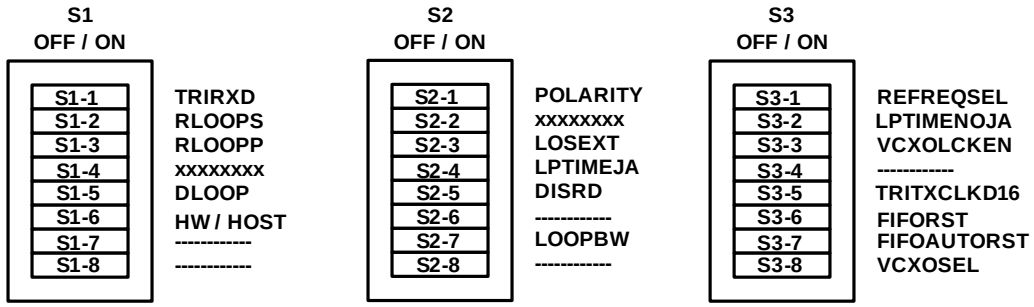
Host mode is enabled from S1 dipswitch and switch number 6. Host mode permits microprocessor control of the XRT91L80 through the Exar supplied **G**raphical **U**ser **I**nterface (GUI) program installed on a **P**ersonal **C**omputer (PC). GUI communication interface are then both provided through the Parallel Port Interface from the PC emulating a simple 4-bit Serial Microprocessor Interface. Other system level components on the evaluation board include **C**lock **M**ultiplier **U**nit (CMU), **C**lock and **D**ata **R**ecovery (CDR), **L**oss **o**f **S**ignal (LOS) detect performance monitoring LEDs. A 155.52 MHz differential crystal oscillator (X1) provides the reference clock needed by the XRT91L80 **P**hase-**L**ocked **L**oop (PLL) components. Evaluation board power is provided through a single power supply banana port connector.

The 3.3V supplies power to the XRT91L80 and a step down power regulator (U7) also provides the 1.8V required by the XRT91L80 core. There are several other optional components for evaluation of supported special features of the XRT91L80 device.

2.1 FUNCTIONALITY AND CONTROL

The three control dipswitches control the function of the XRT91L80. All access to XRT91L80 Hardware Control pins are done through the use of switching these pins to either “high” state or “low” state. Switching to Host Mode permits the Exar supplied XRT91L80 GUI to control and access the XRT91L80 silicon through the 4-bit serial processor interface thereby allowing use of additional features such as performance monitoring and interrupt polling. Host mode overrides the hardware control pins regardless of their logic state.

Figure 2.1 Switch Operation



2.2 XRT91L80 REFERENCE CLOCK

All XRT91L80 boards are shipped with a standard 155.52 MHz differential reference clock oscillator. The 155.52 MHz differential clock oscillator is fed to the XRT91L80’s reference clock inputs REFCLKP/N. The user must then choose the appropriate reference clock frequency setting to properly operate the XRT91L80 based upon the state of ALTFREQSEL pin P1 in Hardware Mode of operation or the logic level of ALTFREQSEL bit in the XRT91L80 software register in Host Mode of operation.

2.3 PARALLEL BUS INTERFACE

OC-48/STM-16 optical signal is received by the optical module and converted to Differential CML electrical signal before being interfaced to the XRT91L80. The XRT91L80 then recovers the clock and data and converts the serial data to SONET/SDH nibble-wide parallel data and outputs both the data and the recovered divide-by-four clock that is synchronous to the parallel data through the received SMB connectors. Both the transmit and the received differential parallel bus interface SMB connectors permit access and connection to a terminal end unit such as a Parallel Bit Error Tester. It also allows a system level remote loopback function, where the received nibble-wide data coming from the XRT91L80 is looped back using high quality SMB coax cables to the nibble-wide transmit input interface of the XRT91L80. Optional 100 Ohm external termination resistors permit the flexibility of connecting/terminating as desired by the user.

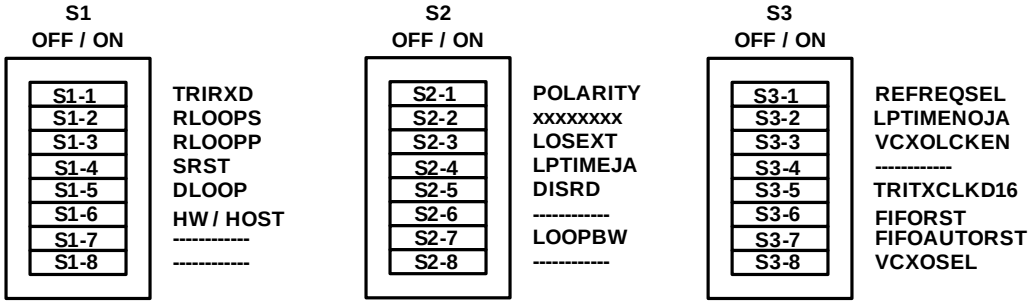
3.0 HARDWARE CONTROL SWITCH DESCRIPTION

There are 3 hardware control dipswitches available to the user on the XRT91L80 Evaluation Board. These switches are used to configure the XRT91L80 into Hardware Mode of Operation. They also provide direct access to XRT91L80 hardware control pins to permit transceiver provisioning as desired by the user. However, some XRT91L80 features like interrupt polling and performance monitoring will not be available in Hardware Mode.

Switch Description:

The three hardware control dipswitches are simply labeled S1, S2, and S3. Each switch within S1, S2 and S3 has a switch number and has been given names appropriate to the pin they control on the XRT91L80. Each switch is defined in details by each table below. An orientation of switch location and their corresponding function is also given. You may find some switch with names on the board silk screen that are not supported on the XRT91L80, these are indicated by a blank line in the diagram below. These switches should be ignored.

Figure 3.0 XRT91L80 Hardware Control Dipswitches



Switch Definition:

Table 1.0 Dipswitch S1

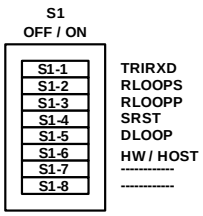
Dipswitch S1	Switch Location	Name	Description
	S1-1	TRIRXD	XRT91L80 hardware pin C12 Parallel Data Output Disable OFF = Normal Mode ON = RXDO[3:0] Data Output Disabled
	S1-2	RLOOPS	XRT91L80 hardware pin C10 Serial Remote Loopback OFF = Normal Mode ON = Enabled
	S1-3	RLOOPP	XRT91L80 hardware pin A11 Parallel Remote Loopback OFF = Normal Mode ON = Enabled
	S1-4	SRST	XRT91L80 hardware pin B10 OFF = Normal Mode ON = Master Reset Asserted
	S1-5	DLOOP	XRT91L80 hardware pin B6 Digital Local Loopback OFF = Normal Mode ON = Enabled
	S1-6	HW / HOST	XRT91L80 hardware pin C9 Host Mode Select Hardware Mode Host Mode/Serial Microprocessor Interface Enabled
	S1-7	xxxxxxxx	
	S1-8	xxxxxxxx	

Table 1.1 Dipswitch S2

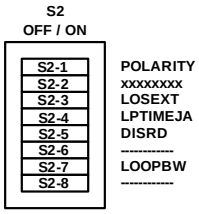
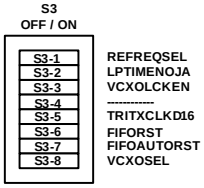
Dipswitch S2	Switch Location	Name	Description
	S2-1	POLARITY	XRT91L80 hardware pin C4 Signal Detect Polarity Select Optical Module Signal Detect input is active “Low” Optical Module Signal Detect is active “High”
	S2-2	xxxxxxxx	
	S2-3	LOSEXT	XRT91L80 hardware pin B5 External Signal Detect Input When POLARITY is active “Low” OFF = Normal Mode ON = Artificially Induced LOS condition When POLARITY is active “High” OFF = Artificially Induced LOS condition ON = Normal Mode
	S2-4	LPTIMEJA	XRT91L80 hardware pin C6 Loop timing thru External VCXO Jitter Attenuation OFF = Normal Mode ON = Loop timing using external VCXO de-jittered clock
	S2-5	DISRD	XRT91L80 hardware pin A3 Mute Upon LOSD OFF = Normal Mode ON = Mute RXDO[3:0] upon Loss of Signal Detect
	S2-6	----------	
	S2-7	LOOPBW	XRT91L80 hardware pin M7 PLL bandwidth select: Use Wide Band for lower quality oscillator and Narrow Band for high quality oscillator and improved performance. Wide Band (4x) Narrow Band (1x)
	S2-8	----------	

Table 1.2 Dipswitch S3

Dipswitch S3	Switch Location	Name	Description
	S3-1	REFREQSEL	XRT91L80 hardware pin P1
			Reference Frequency Select 77.76 MHz Reference Frequency Oscillator 155.52 MHz Reference Frequency Oscillator
	S3-2	LPTIMENOJA	XRT91L80 hardware pin P2
			Loop Timing without Jitter Attenuation OFF = Local timing/ Local or loop timing w/ VCXO ON = Loop timing without external VCXO Jitter Attenuation
	S3-3	VCXOLCKEN	XRT91L80 hardware pin P3
			VCXO Lock Enable OFF = Normal Mode ON = VCXO Lock Enable
	S3-4	----------	
	S3-5	TRITXCLKD16	XRT91L80 hardware pin M12
			Auxiliary Clock Disable OFF = Normal Mode ON = TXCLKO16 Disabled
	S3-6	FIFORST	XRT91L80 hardware pin N13
			Manual FIFO Reset OFF = Normal Mode ON = Manual FIFO Reset
	S3-7	FIFOAUTORST	XRT91L80 hardware pin N12
			Auto FIFO Reset OFF = Disabled ON = Enabled
	S3-8	VCXOSEL	XRT91L80 hardware pin M6
			External VCXO select OFF = Normal Mode ON = External VCXO selected for transmit timing

4.0 SETTING UP THE XRT91L80 EVALUATION BOARD FOR HARDWARE TEST

The XRT91L80 Evaluation Board can be used to test both the OC-48 high speed serial interface and the 622.08 Mbps low speed 4-bit parallel bus interface. OC-48 high speed serial interface testing is referred to as SONET/SDH testing and 622.08 Mbps low speed 4-bit parallel bus testing is referred to as Parallel Bit Error testing. The following sections cover the differences in each setup.

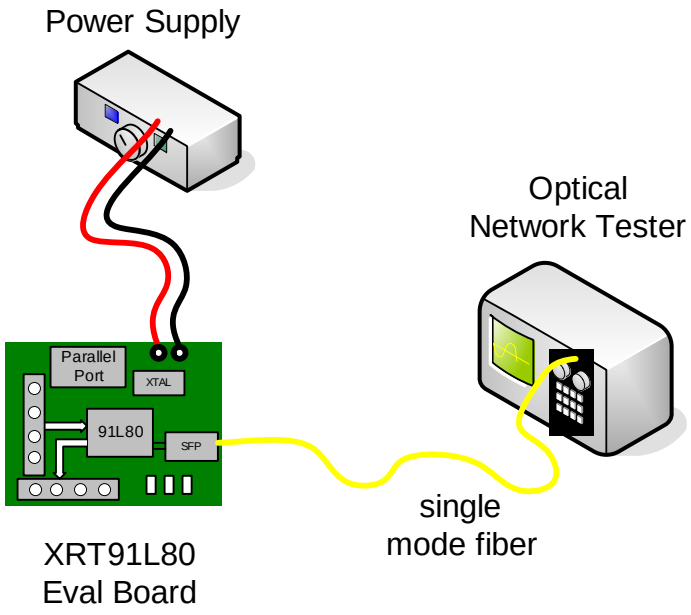
4.1 Setting up the XRT91L80 Evaluation Board for SONET/SDH testing in Hardware Mode
4.2 Setting up the XRT91L80 Evaluation Board for Parallel Bit Error testing in Hardware Mode

4.1 SETTING UP THE XRT91L80 EVALUATION BOARD FOR SONET/SDH TESTING

To successfully perform this test, you must have the following equipment:

- XRT91L80 Evaluation Board
- 3.3V Power Supply capable of delivering1 amp.
- An optical SONET/SDH test equipment
- An optical attenuator if necessary

Figure 4.0 Hardware Mode SONET/SDH Transceiver Test Setup

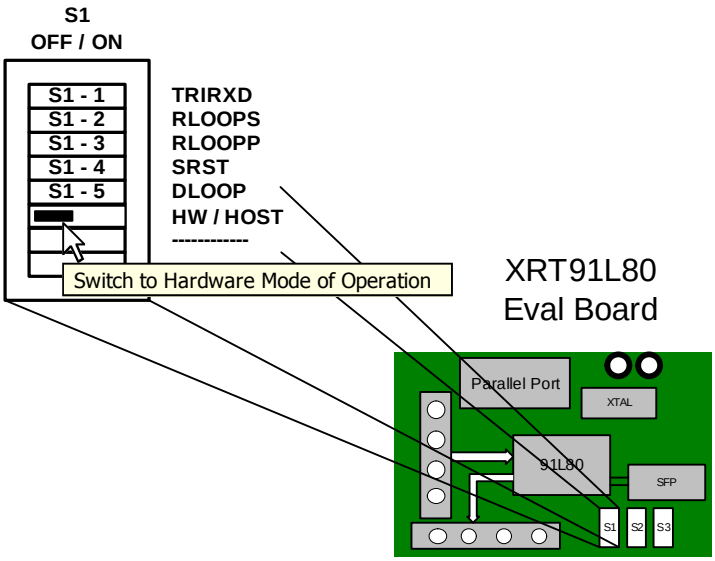


Startup procedure:

1. Adjust and verify 3.3V power supply with a Voltmeter. Connect 3.3V power supply to board using banana leads.
2. Turn on power and verify power supply on the board by checking Power LED.
3. Connect the optical cable from the OC-48/STM-16 SFP module to the Optical Network Test Equipment. Verify optical signal strength and attached an optical attenuator to the receiver end of the test equipment if necessary.

4. Verify that Dipswitch 1 switch 6 (S1-6) is in the Hardware position according to the diagram below (switch on left side). Note: The silkscreen on the board is incorrect. Follow Figure 4.1 below for the correct position.

Figure 4.1 Hardware Mode Position



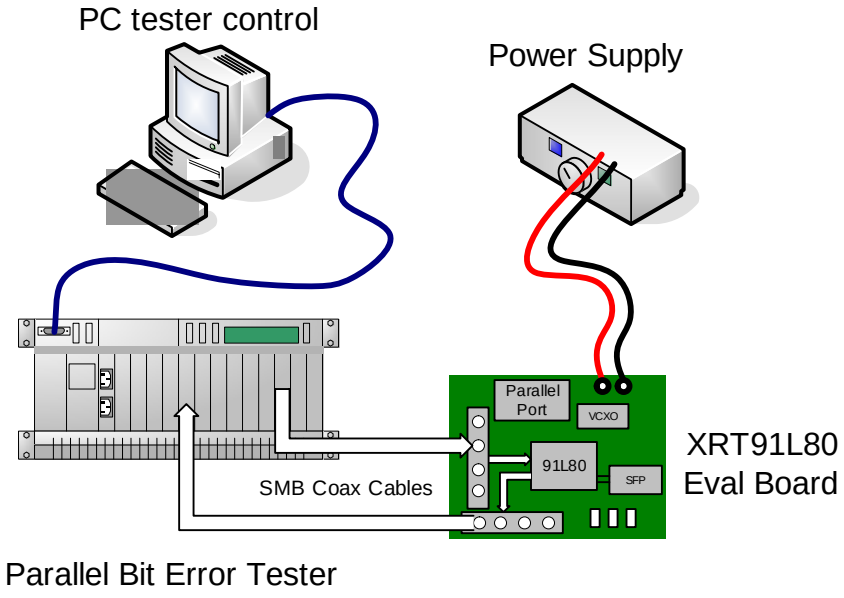
5. Configure the XRT91L80 Hardware pins using the 3 dipswitches for proper operation. See section 5.0, “Configure the XRT91L80 for proper operation in Hardware Mode.”

4.2 SETTING UP THE XRT91L80 EVALUATION BOARD FOR PARALLEL BIT ERROR TESTING

To successfully perform this test, you must have the following equipment:

- XRT91L80 Evaluation Board
- 3.3V Power Supply capable of delivering1 amp.
- An electrical Parallel Bit Error test equipment
- A PC to control the Parallel Bit Error test equipment
- 20 high quality SMB coax cables for parallel bus connection

Figure 4.2 Hardware Mode Parallel Bit Error Test Transceiver Test Setup

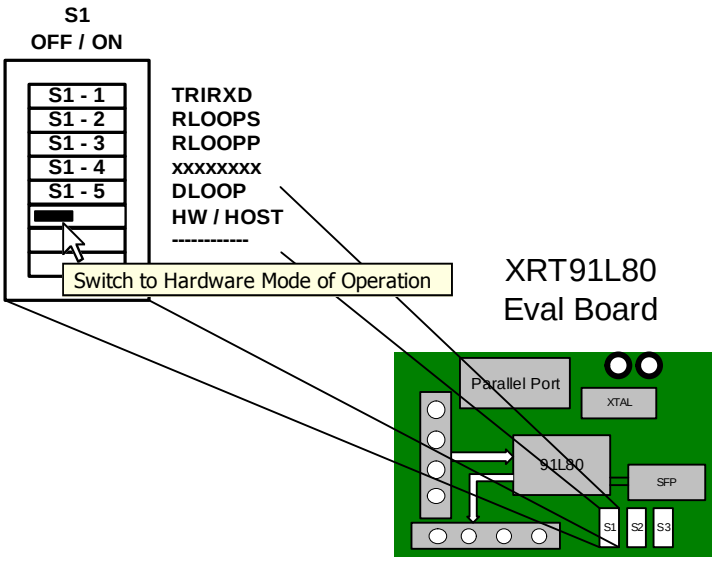


Startup procedure:

1. Adjust and verify 3.3V power supply with a Voltmeter. Connect 3.3V power supply to board using banana leads.
2. Turn on power and verify power supply on the board by checking Power LED.
3. Connect the SMB cables to the parallel bus interface SMB connectors and to the appropriate test equipment port connector. At a minimum, 10 cables will be needed for TXDI[3:0]P/N and TXPCLKIP/N differential transmit parallel bus interface and another 10 cables are needed for RXDO[3:0]P/N and RXPCLKOP/N differential receive parallel bus interface.

4. Verify that Dipswitch 1 switch 6 (S1-6) is in the Hardware position according to the diagram below (switch on left side). Note: The silkscreen on the board is incorrect. Follow Figure 4.1 below for the correct position.

Figure 4.3 Hardware Mode Position

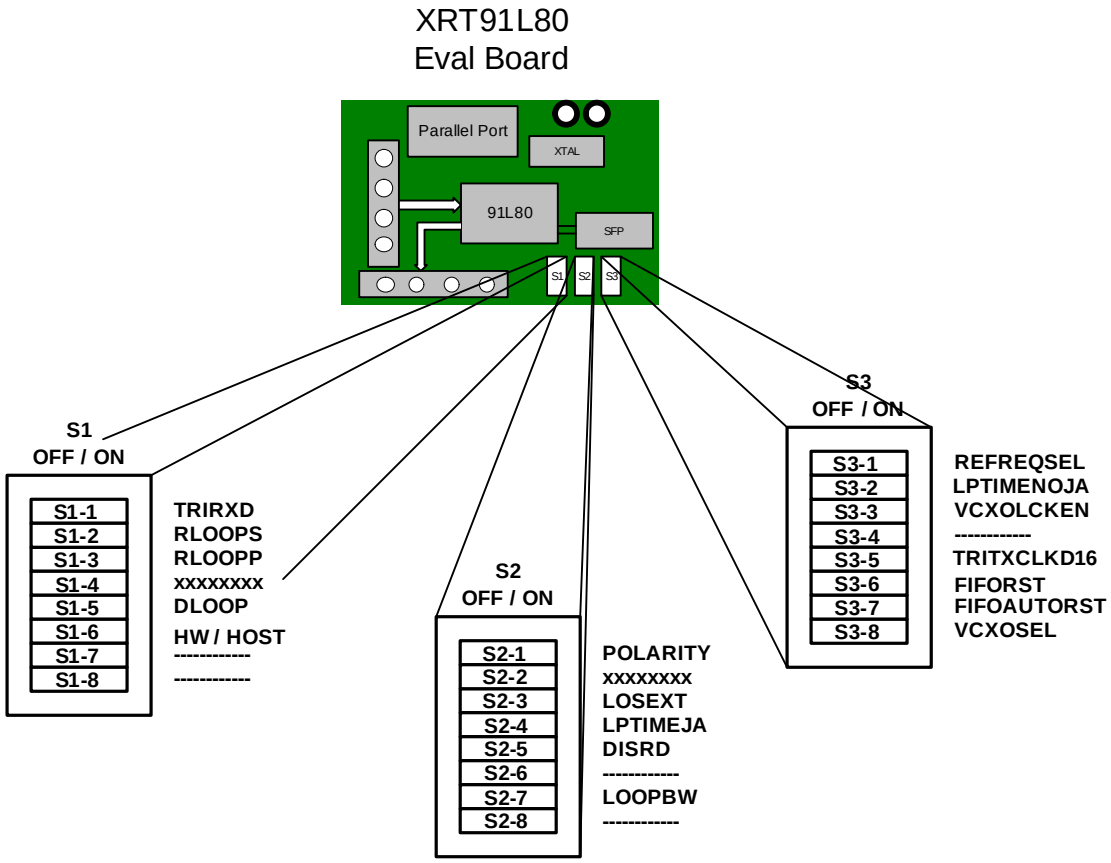


5. Configure the XRT91L80 Hardware pins using the 3 dipswitches for proper operation. See section 5.0, “Configure the XRT91L80 for proper operation in Hardware Mode.”

5.0 CONFIGURING THE XRT91L80 FOR PROPER OPERATION IN HARDWARE MODE

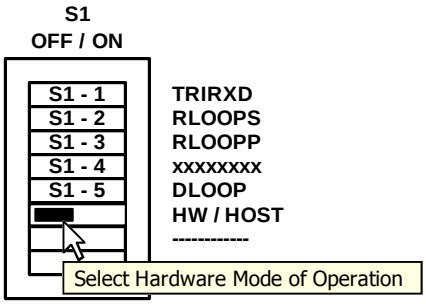
In Hardware mode, the XRT91L80 will require pins to be properly configured to function properly. Below is a diagram that shows the relative location of the three dipswitches S1, S2, and S3 on the evaluation board that control the hardware pins on the XRT91L80.

Figure 5.0 Hardware Control Switch Locations



Step 1. To operate in Hardware Mode, The HW/Host Mode must **always** be in the correct position. Select Hardware Mode.

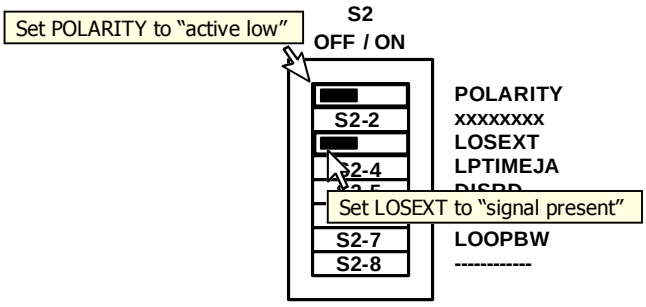
Figure 5.1 Select Hardware Mode



Note: The silkscreen on the board is incorrect. Follow Figure 5.1 above for the correct position.

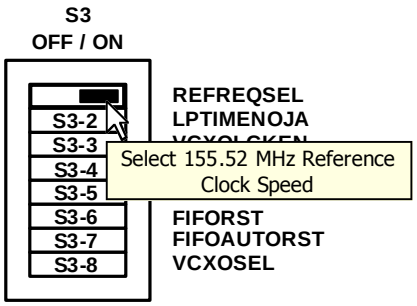
Step 2. Under normal circumstances, LOSEXT is connected to the optical module and POLARITY is set according to optical module Loss of Signal (LOS) detect convention. However the evaluation board does not connect these pins to the optical module or hardwire POLARITY to permit evaluation and manipulation through the control switches. These pins must be set correctly to prevent unintentional LOS assertion. Verify the correct switch position for POLARITY and LOSEXT. By default, the POLARITY and LOSEXT pins have been set to active “low” and signal “present” respectively and according to the diagram below. Set the switches according to the diagram below for normal operation. See dipswitch definition in section 3.0, Table 1.1 Dipswitch S2 for a full description.

Figure 5.2 POLARITY and LOSEXT Convention



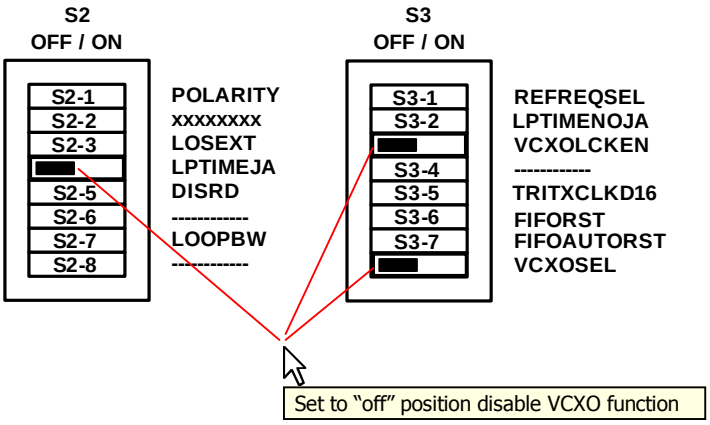
Step 3. XRT91L80 Evaluation Boards are shipped with a standard 155.52 MHz reference clock oscillator. REFREQSEL should be set to the right side by default indicating a 155.52 MHz reference clock speed selection.

Figure 5.3 Select 155.52 MHz Reference Frequency



Step 4. The XRT91L80 evaluation board has provisions for the operation of a Voltage Controlled External Oscillator. However, the XRT91L80 does not require the operation of a Voltage Controlled External Oscillator. Disable all VCXO functionality pins.

Figure 5.4 Disable All VCXO functional pins



Step 5. You are now ready to execute the XRT91L80's features and functions.

6.0 XRT91L80 EXAMPLE APPLICATIONS USING HARDWARE MODE

The following example applications are provided in this manual using Hardware Mode.

6.1 Diagnostic Loopback Operations
- 6.1.1 Remote Serial Loopback
- 6.1.2 Remote Parallel Loopback
- 6.1.3 Bit Error Test Using Local Digital Loopback

6.2 Master Reset

6.1 DIAGNOSTIC LOOPBACK OPERATIONS

Loopback operations generally fall under two different categories and are referenced with respect to the device. Remote loopback and Local Loopback are both available on the XRT91L80 device. Remote Loopback indicates that remote equipment (test equipment) signal is routed back to the equipment. Hence, all types of remote loopback routes received signal back to the transmit side. Local loopback indicates that link layer or terminal equipment signal (hence, local signal) is routed back to the link layer or terminal equipment. This means locally transmitted signal is routed back to the receiver.

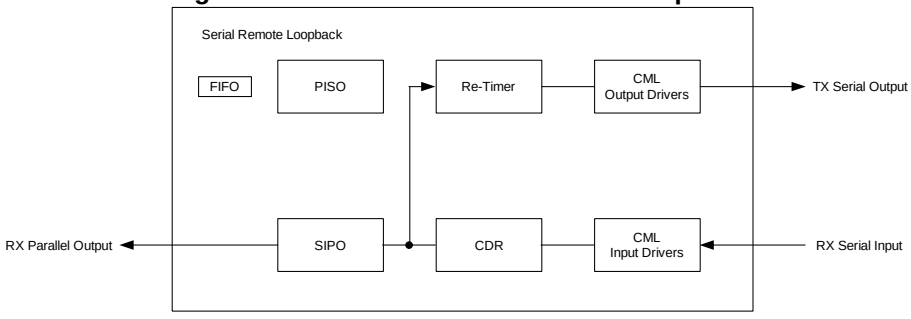
There are a total of three types of loopback operations available on the XRT91L80.
Two of the loopbacks are remote equipment loopback and one is a local terminal equipment loopback:

- Remote Serial Loopback
- Remote Parallel Loopback
- Local Digital Loopback

6.1.1 Remote Serial Loopback

Remote serial loopback on the XRT91L80 can be implemented to quickly determine OC-48 test equipment line integrity. The figure below exemplifies this type of loopback and the data paths.

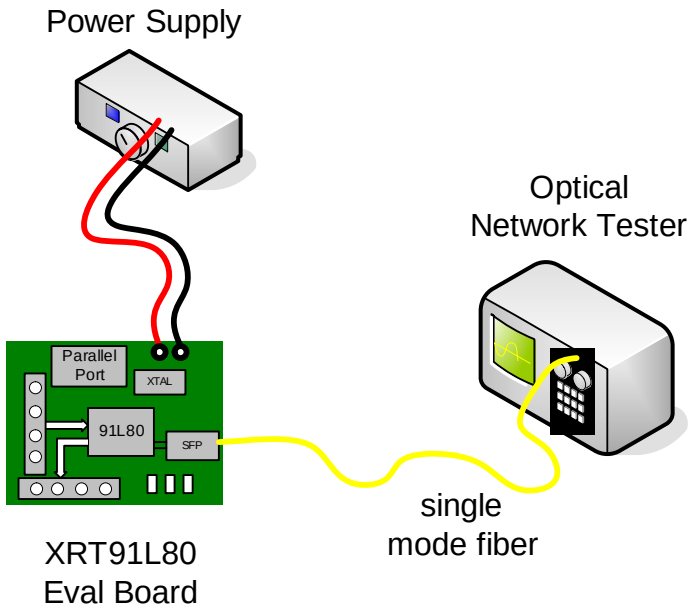
Figure 6.0 XRT91L80 Remote Serial Loopback



Hardware Configuration for Remote Serial Loopback Operation

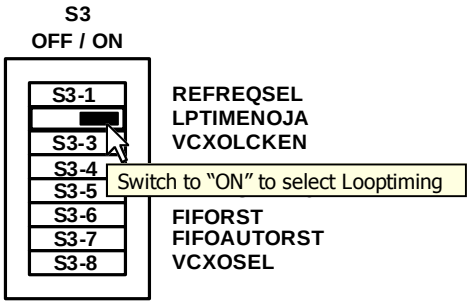
Step 1. Set up the XRT91L80 Evaluation Board as outlined in section 4.1, “Setting up the XRT91L80 Evaluation Board for SONET/SDH Testing in Hardware Mode.” Follow the instructions on section 5.0, “Configuring the XRT91L80 for proper operation in Hardware Mode.” Once you have configured the XRT91L80 to the proper settings, you are now ready to invoke the XRT91L80 features.

Figure 6.1 Hardware Mode SONET/SDH Test Setup



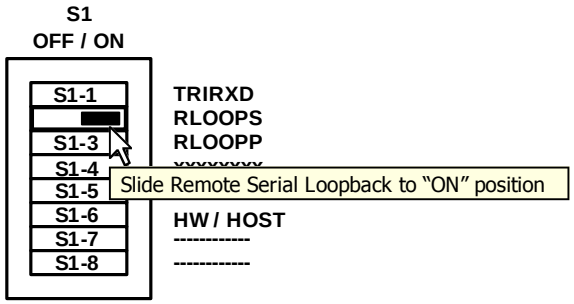
Step 2. Select **Looptiming** mode for the XRT91L80 transmit timing.

Figure 6.2 Select Looptiming



Step 3. To put the XRT91L80 in remote serial loopback operation, move the RLOOPS switch to the ON position (switch to right side) on Dipswitch 1 switch 2 (S1-2) shown below.

Figure 6.3 Enable Remote Serial Loopback



Step 4. Check test equipment for valid pattern synchronization.

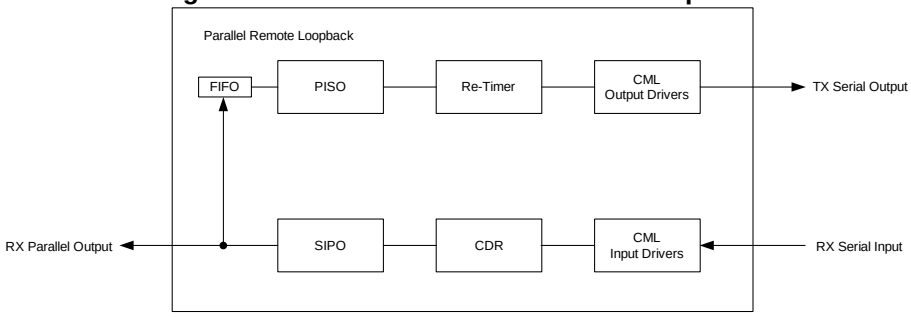
Note: If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and re-verify data integrity.

Step 5. To return to normal operation, move the switch to the OFF position (switch to the left side) on Dipswitch 1 switch 2 (S1-2).

6.1.2 Remote Parallel Loopback

Remote parallel loopback on the XRT91L80 can be implemented to quickly determine OC-48 test equipment line integrity. This type of loopback is essentially a parallel cable remote loopback with the exception that the loopback is routed internally within the XRT91L80. In addition, it also sends the received parallel data to the received parallel bus interface. The figure below exemplifies this type of loopback and the data paths.

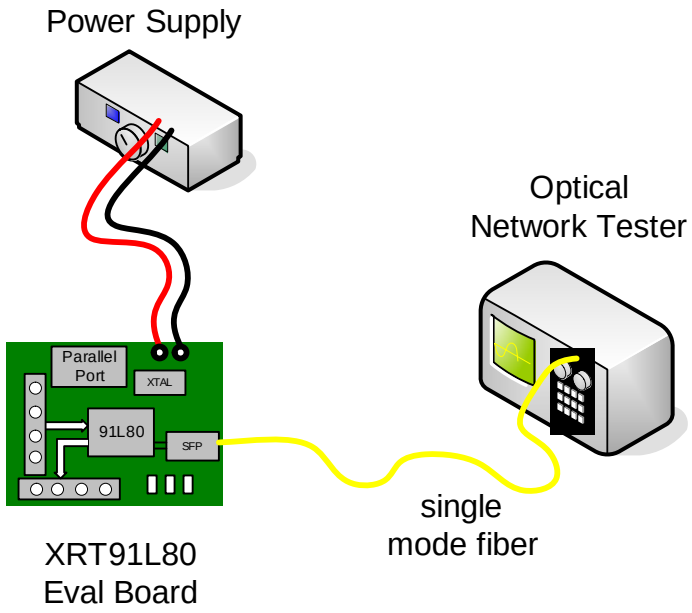
Figure 6.4 XRT91L80 Remote Parallel Loopback



Hardware Configuration for Remote Parallel Loopback Operation

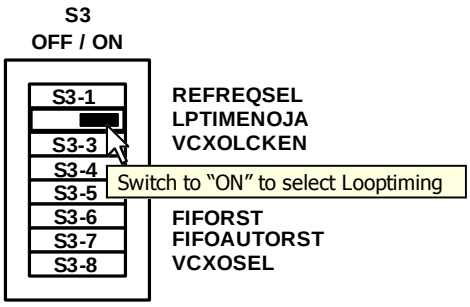
Step 1. Set up the XRT91L80 Evaluation Board as outlined in section 4.1, “Setting up the XRT91L80 Evaluation Board for SONET/SDH Testing in Hardware Mode.” Follow the instructions on section 5.0, “Configuring the XRT91L80 for proper operation in Hardware Mode.” Once you have configured the XRT91L80 to the proper settings, you are now ready to invoke the XRT91L80 features.

Figure 6.5 Hardware Mode SONET/SDH Test Setup



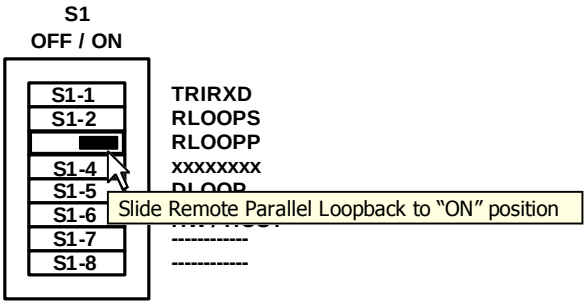
Step 2. Select **Looptiming** mode for the XRT91L80 transmit timing.

Figure 6.6 Select Looptiming



Step 3. To put the XRT91L80 in remote parallel loopback operation, move the RLOOPP switch to the ON position (switch to right side) on Dipswitch 1 switch 3 (S1-3) shown below.

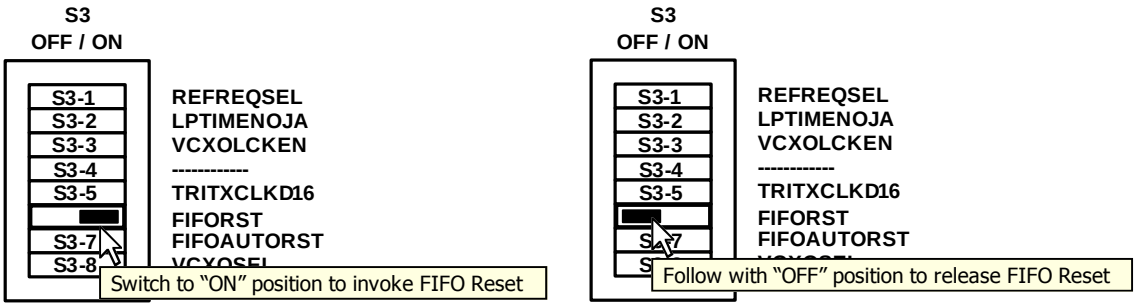
Figure 6.7 Enable Remote Parallel Loopback



IMPORTANT: Switching to remote parallel loopback operation sends the received parallel data to the transmit parallel data thru the transmit FIFO. Examine Figure 6.4 "Remote Parallel Loopback" block diagram. Therefore, the FIFORST switch must also be toggled to flush the FIFO whenever the remote parallel loopback is enabled. To flush the FIFO, move the switch on the FIFORST to the ON position (switch to the right side) on Dipswitch 3 switch 6 (S3-6) followed by returning the switch to the OFF position (switch to the left side).

Step 4. Invoke a manual FIFO Reset to flush the FIFO.

Figure 6.8 Manual FIFO Reset

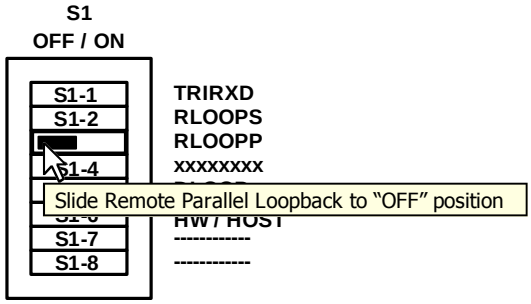


Step 5. Check test equipment for valid pattern synchronization.

Note: If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and re-verify data integrity.

Step 6. To return to normal operation and remove Remote Parallel Loopback, move the switch to the OFF position (switch to the left side) on Dipswitch 1 switch 3 (S1-3).

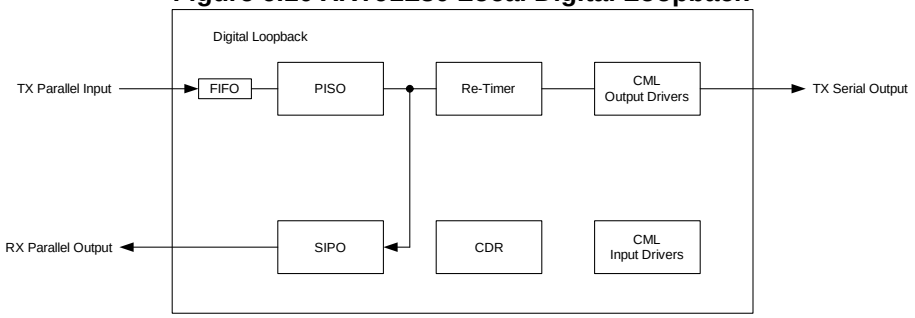
Figure 6.9 Disable Remote Parallel Loopback



6.1.3 Bit Error Test Using Local Digital Loopback

This loopback needs to be invoked whenever local diagnostic is desired or as such when a Parallel Bit Error Tester or a Parallel bit generator and analyzer is used. Local transmit data is looped-back at the Parallel-Input to Serial-Output (PISO) Block to the Serial-Input to Parallel-Output (SIPO) Block. Local digital loopback on the XRT91L80 can be implemented to quickly determine line integrity up to the transceiver. The figure below exemplifies this type of loopback and the data path.

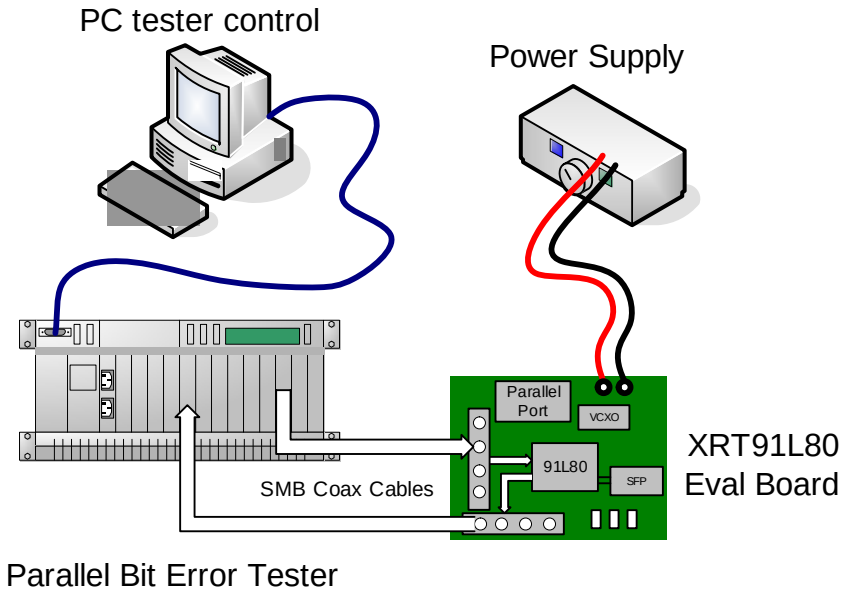
Figure 6.10 XRT91L80 Local Digital Loopback



Hardware Configuration for Bit Error Test Using Local Digital Loopback Operation

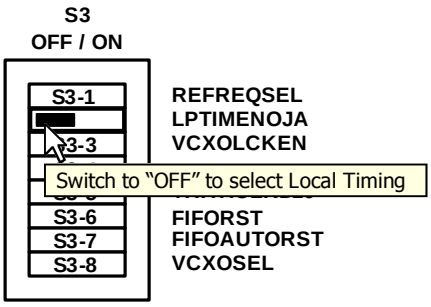
Step 1. Set up the XRT91L80 Evaluation Board as outlined in section 4.2, "Setting up the XRT91L80 Evaluation Board for Parallel Bit Error Testing in Hardware Mode." Use high quality SMB coax cables to connect the Parallel Bit Error Tester to the XRT91L80 Evaluation Board. Once your setup is ready, follow the instructions on section 5.0, "Configuring the XRT91L80 for proper operation in Hardware Mode." After you have configured the XRT91L80 to the proper settings, you are now ready to invoke the XRT91L80 features.

Figure 6.11 Parallel Bit Error Test Setup



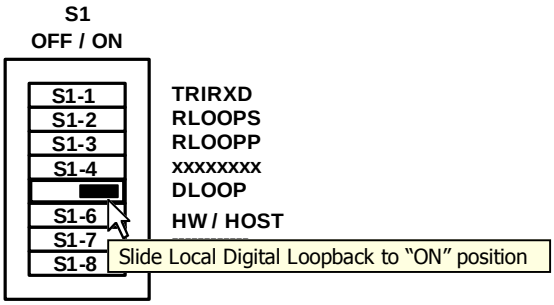
Step 2. Select **Local Timing** mode for the XRT91L80 transmit timing.

Figure 6.12 Select Local Timing



Step 3. To put the XRT91L80 in local digital loopback operation, move the DLOOP switch to the ON position (switch to right side) on Dipswitch 1 switch 5 (S1-5) shown below.

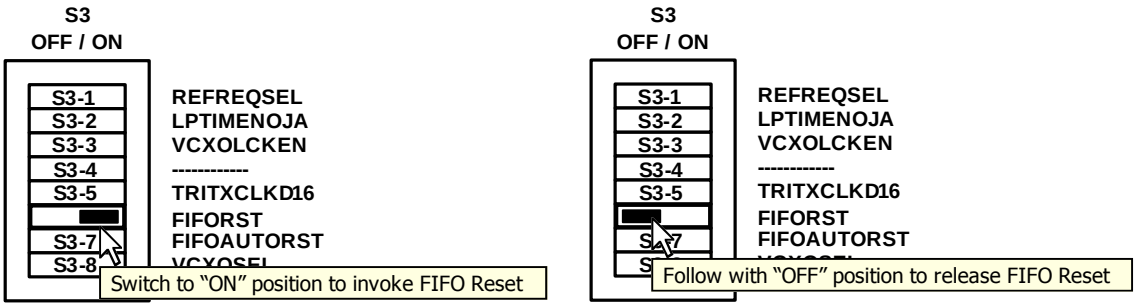
Figure 6.13 Enable Local Digital Loopback



IMPORTANT: Switching to local digital loopback operation sends the transmit parallel data to the received parallel data thru the transmit FIFO. Examine Figure 6.10 "Local Digital Loopback" block diagram. Therefore, the FIFORST switch must also be toggled to flush the FIFO whenever the local digital loopback is enabled. To flush the FIFO, move the switch on the FIFORST to the ON position (switch to the right side) on Dipswitch 3 switch 6 (S3-6) followed by returning the switch to the OFF position (switch to the left side).

Step 4. Invoke a manual FIFO Reset to flush the FIFO.

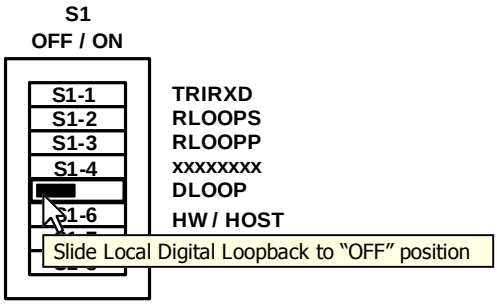
Figure 6.14 Manual FIFO Reset



Step 5. Begin Parallel Bus transmission and Bit Error Test and check the test equipment for valid pattern synchronization.

Step 6. To remove Local Digital Loopback, move the switch to the OFF position (switch to the left side) on Dipswitch 1 switch 5 (S1-5).

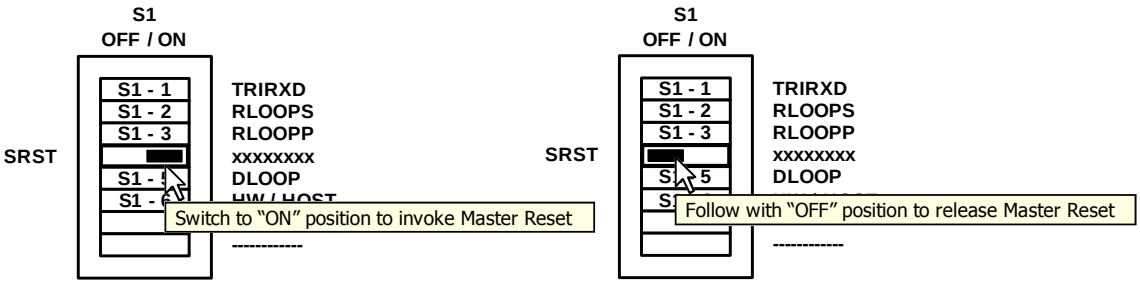
Figure 6.15 Disable Local Digital Loopback



6.2 MASTER RESET

Whenever necessary, the XRT91L80 can be reset. To invoke this, toggle the switch of the Master Reset pin by sliding the switch of the SRST to the ON position (switch to the right side) on Dipswitch 1 switch 4 (S1-4) followed by returning the switch to the OFF position (switch to the left side). This will toggle the hardware reset pin on the XRT91L80.

Figure 6.16 Master Reset



7.0 INSTALLING THE XRT91L80 EVALUATION GUI

To install the XRT91L80 GUI, double click on the installation file enclosed in the CD, as part of the evaluation package. This will place the relevant GUI files in an Exar created folder.

7.1 STARTING THE EVALUATION SOFTWARE

The evaluation software allows the user to do the following:

- Configure the XRT91L80 for proper operation
- Poll current alarm status.
- Enable/Disable XRT91L80 features with the click of a button

Once the XRT91L80 GUI is installed, it can be found through the **Start Menu->Exar->XRT91L80 Evaluation**. Once selected, it will open up the application. To begin the GUI, select **Test** from the menu bar and then **Start XRT91L80**. This will bring up the dialog box on the next page.

Figure 7.1 Start Test

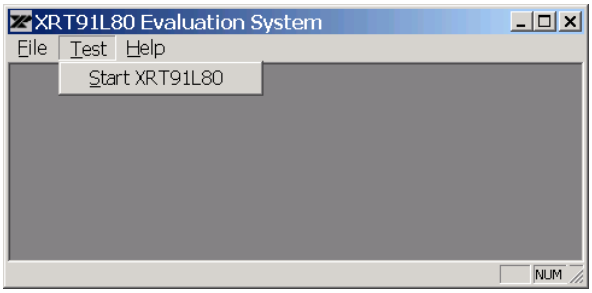
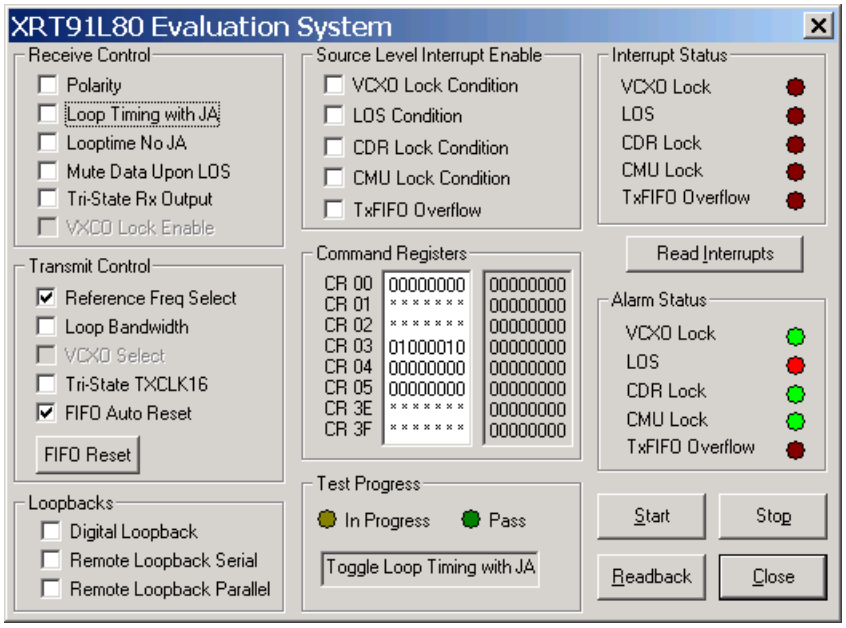


Figure 7.2 Main GUI Window



Make sure the following are correct:

1. Connect the power supply to the board (all power is derived on board from the 3.3 volt supply.
2. Connect the PC to the board with the parallel port cable.
3. Connect an optical cable to the SFM module from a signal source.
4. Power up the system and verify that the PC to XRT91L80 communications are working.

7.2 GUI Block Description

Source Level Interrupt Enable (Reg 0x00):
This register allows the user to enable or disable interrupts on the xrt91L80.

Transmit Control (Reg 0x03):
This register allows the user to control the output signal.

Receive Control (Reg 0x04):
This register allows the user to control the input signal.

Channel Control (Reg 0x05):
This register has the loopback selections.

Interrupt Status (Reg 0x01):
This register reflects the interrupts that occur.

Alarm Status (Reg 0x02):
This register reflects the alarms that occur.

Command Registers:
This section reflects the selections chosen. The user can see what is being written to the device, and the corresponding alarm/interrupt registers.

7.3 BUTTON DESCRIPTIONS

Start:
This button will start the polling test of the XRT91L80.

Stop:
This button will stop the polling test of the XRT91L80.

Readback:
This button reads out all the registers in the XRT91L80 and the results are displayed in the Command Registers section.

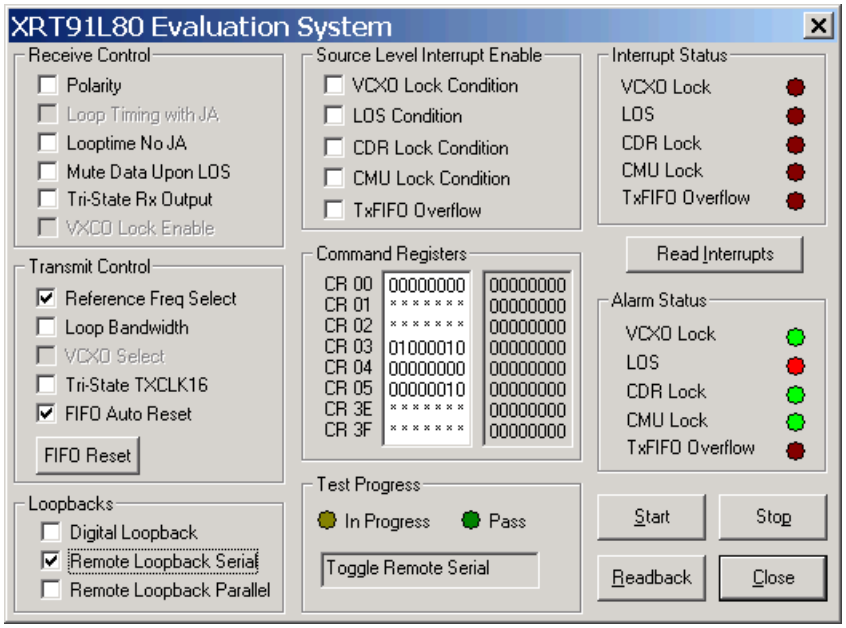
Reset:
Resets the software registers of the XRT91L80.

Read Interrupts:
Reads the interrupt register and displays an interrupt (alarm will light up) in the interrupt status section when an interrupt occurs.

7.4 REMOTE SERIAL LOOPBACK USING GUI

Set the XRT91L80 into the remote (serial) loopback mode and verify that the board is receiving and transmitting data. Figure 7.3 indicates the selection.

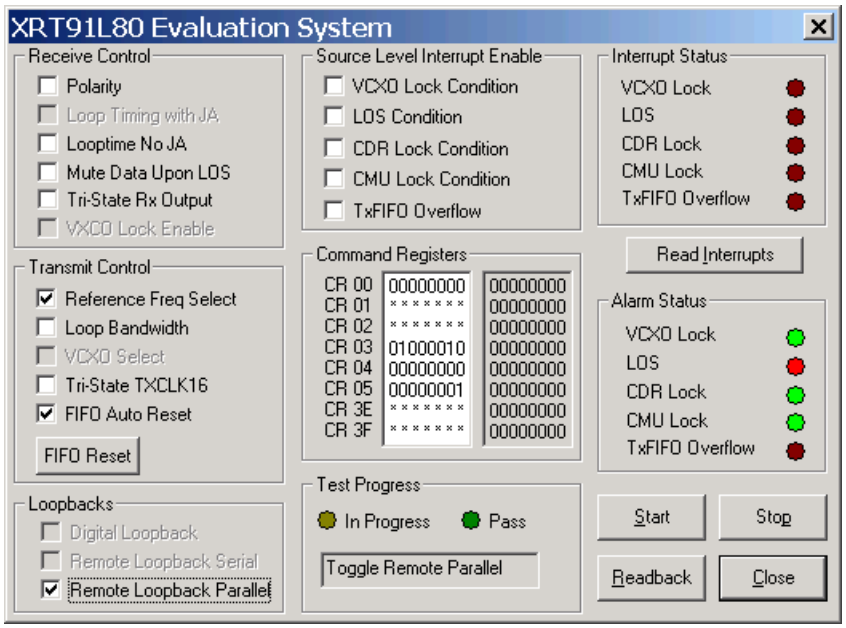
Figure 7.3 GUI with Remote Serial Loopback Enabled



7.5 REMOTE PARALLEL LOOPBACK USING GUI

Remove the serial loopback and select the “Remote parallel” loopback mode. See Figure 7.4

Figure 7.4 Serial loopback disabled and “Remote parallel” loopback selected

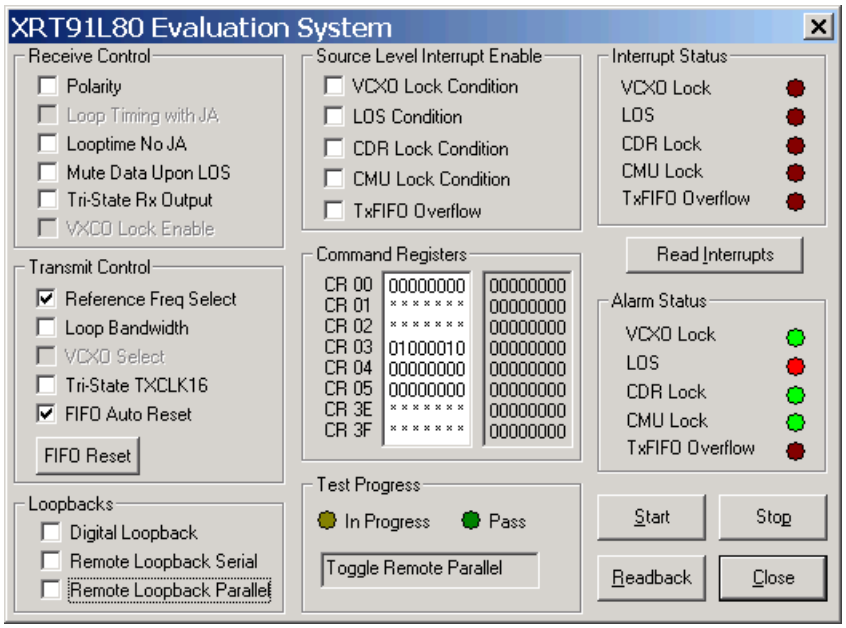


Note: After starting test, the “FIFO Reset” should be activated (and deactivated) to Flush the FIFO.

7.6 EXTERNAL LOOPBACK USING GUI

Switch to external loopback (disable Remote loopback mode) and verify that the data flows out of the receive section, through the cables from the RXDn pins to the TXDn pins, and back out the transmit section to the test equipment. See Figure 7.5.

Figure 7.5 External Loopback mode

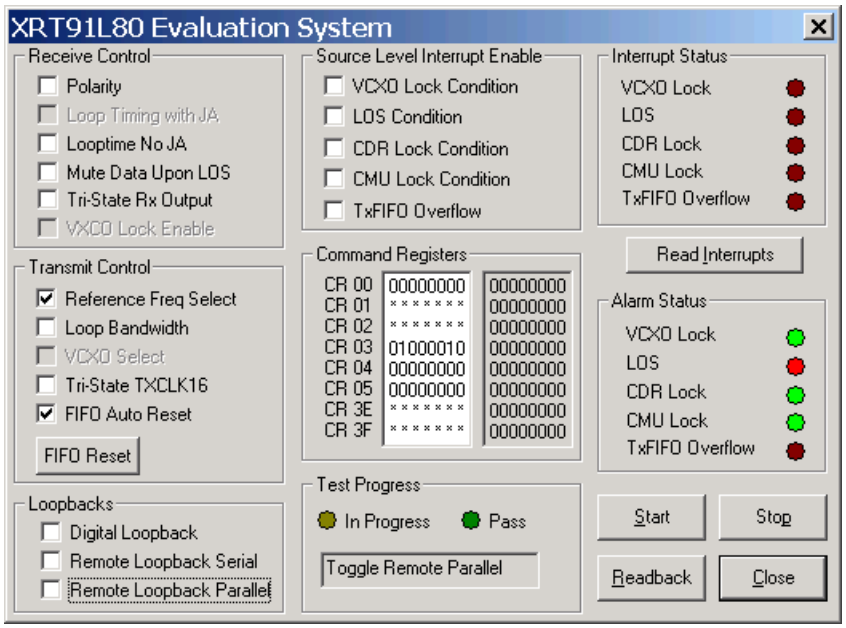


Note: After starting test, the “FIFO Reset” should be activated (and deactivated) to Flush the FIFO.

7.7 TX/RX RUNNING INDEPENDENT USING GUI

No loopback mode (Tx and Rx running independent) is shown in Figure 7.6.

Figure 7.6 TX & RX w/ REFCLK @ 155.52 MHz



Note: After starting test, the "FIFO Reset" should be activated (and deactivated) to Flush the FIFO.

8.0 CONFIGURING THE XRT91L80 EVALUATION BOARD FOR JITTER MEASUREMENTS

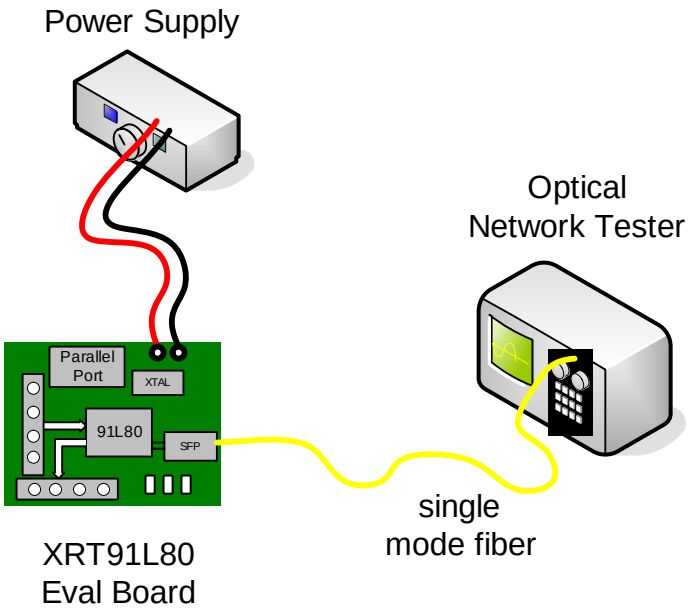
There are three types of jitter measurement of interest in the XRT91L80 transceiver product. They are received jitter tolerance, jitter transfer, and transmit intrinsic jitter.

- How to measure optical Jitter Tolerance of the XRT91L80
- How to measure optical Jitter Transfer of the XRT91L80
- How to measure optical Intrinsic Jitter of the XRT91L80

Since the XRT91L80 Evaluation Board uses an optical interface, a network tester with an optical interface capable of jitter measurements will be required to successfully characterize optical jitter performance on the XRT91L80. Below is a simple diagram of the jitter measurement setup.

To simplify the test setup, all are jitter test setup are shown using Hardware Mode on the XRT91L80. However, the user can use Host mode to perform all the jitter test and measurement.

Figure 8.0 Jitter Measurement Setup



8.1 HOW TO MEASURE OPTICAL JITTER TOLERANCE OF THE XRT91L80

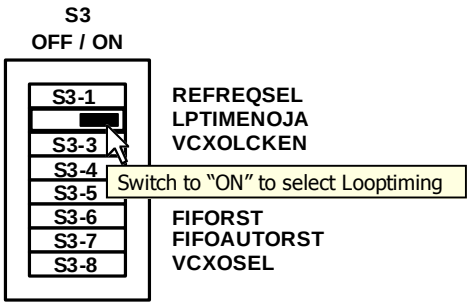
To successfully perform this test, the user needs to configure the XRT91L80 into:

- Remote Serial Loopback
- Looptiming

Step 1. Configure the XRT91L80 for Remote Serial Loopback as outlined in section 6.1.1, “Remote Serial Loopback.”

Step 2. Select **Looptiming** mode for the XRT91L80 transmit timing.

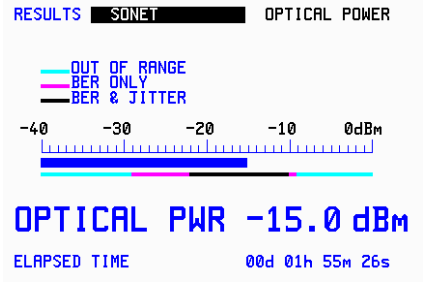
Figure 8.1 Select Looptiming



Step 3. Select the proper SONET/SDH data rate source and payload pattern on test equipment and verify recovered data integrity and pattern sync on test equipment.

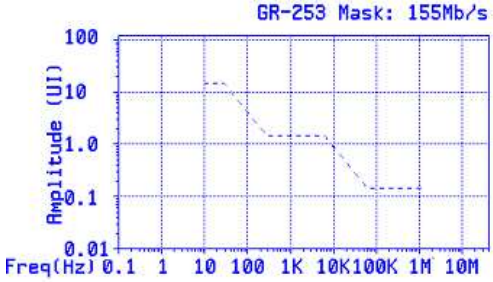
Step 4. Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler/connector until desired optical signal strength is achieved for valid jitter measurements.

Figure 8.2 Optical Signal Strength (Test Equipment)



Step 5. Configure the test equipment for Jitter Tolerance measurements and select the appropriate Jitter Tolerance Mask Standard for SONET STS-48/SDH STM-16.

Figure 8.3 GR.253 Jitter Tolerance Mask (Test Equipment)



Step 6. Begin Jitter Tolerance Measurements.

8.2 How to measure Optical Jitter Transfer of the XRT91L80

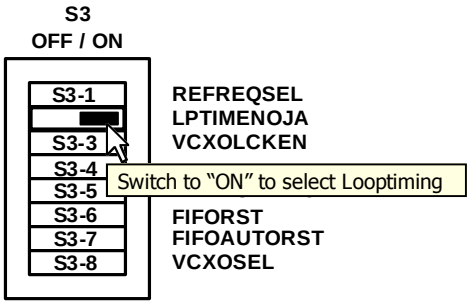
To successfully perform this test, the user needs to configure the XRT91L80 into:

- Remote Serial Loopback
- Looptiming

Step 1. Configure the XRT91L80 for Remote Serial Loopback as outlined in section 6.1.1, "Remote Serial Loopback."

Step 2. Select **Looptiming** mode for the XRT91L80 transmit timing.

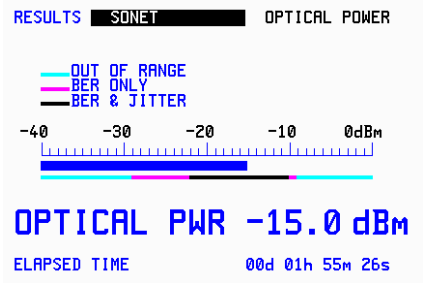
Figure 8.4 Select Looptiming



Step 3. Select the proper SONET/SDH data rate source and payload pattern on test equipment and verify recovered data integrity and pattern sync on test equipment.

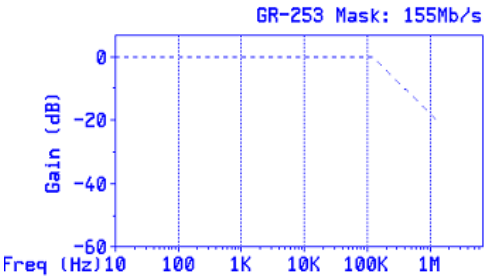
Step 4. Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler/connector until desired optical signal strength is achieved for valid jitter measurements.

Figure 8.5 Verify Optical Signal Strength (Test Equipment)



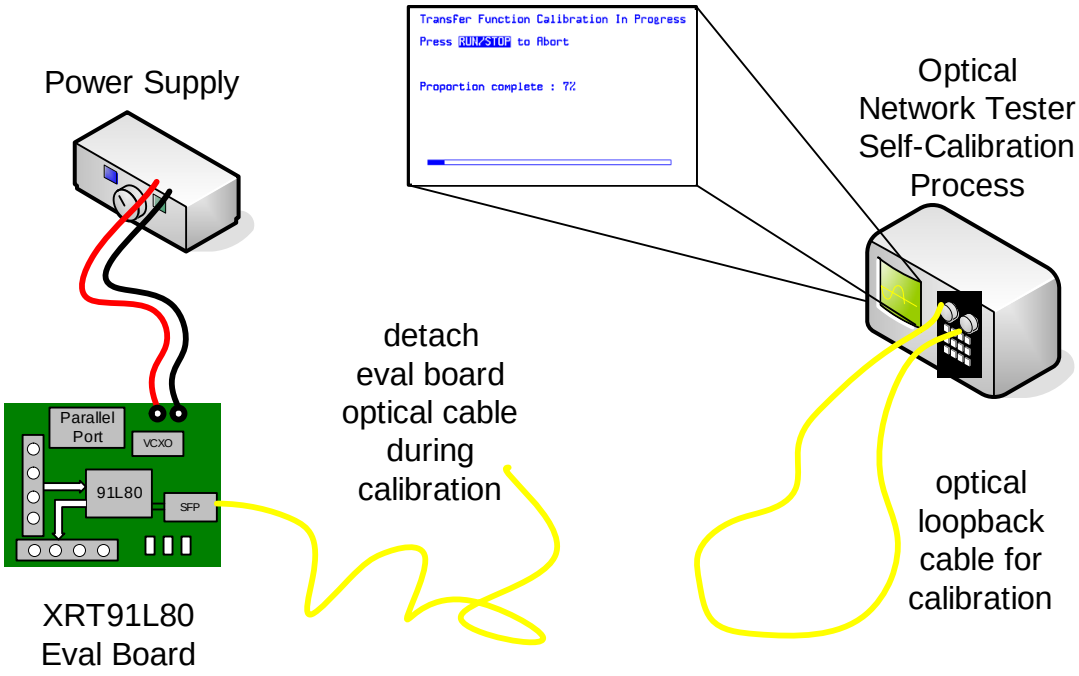
Step 5. Configure the test equipment for Jitter Transfer measurements and select the appropriate Jitter Transfer Mask Standard for SONET STS-48/SDH STM-16.

Figure 8.6 GR.253 Jitter Transfer Mask (Test Equipment)



Step 6. Most test equipment will require an initial jitter transfer calibration before proceeding with jitter transfer measurements. Therefore, detach the Evaluation Board connected optical cable from the test equipment and replace a with an optical loopback cable for the calibration process. Follow test equipment instructions for calibration and do not interrupt calibration process.

Figure 8.7 Jitter Transfer Calibration (Test Equipment)



Step 7. Once initial calibration is done, replace the optical loopback cable on the test equipment with the Evaluation Board optical cable. Verify that transmit and receive cables are properly oriented and test equipment receiver does not declare Loss of Signal. Once Evaluation Board optical cable is inserted and data integrity and pattern sync is achieved, verify that the optical signal strength is valid for jitter measurements before proceeding to the next step.

Figure 8.8 Reattach Evaluation Board optical cable

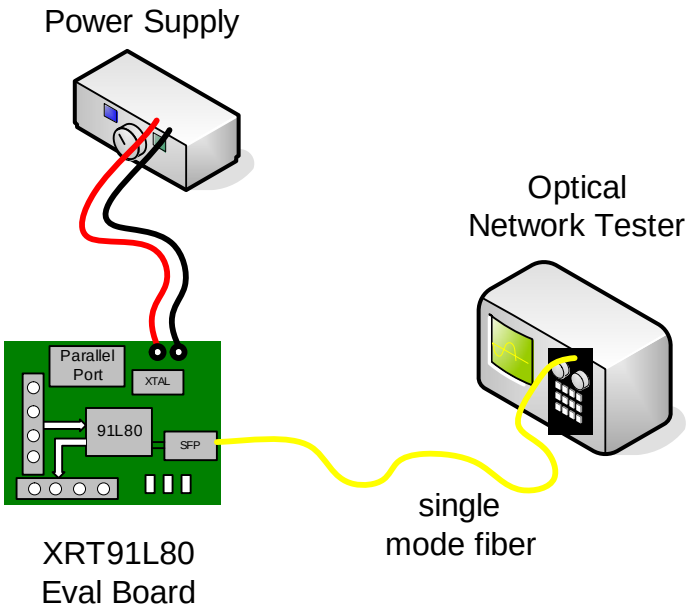
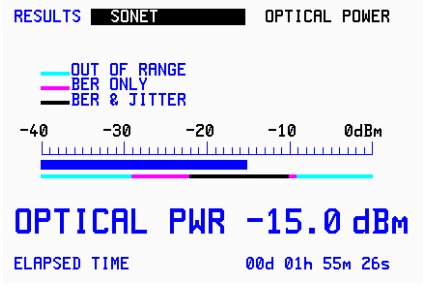


Figure 8.9 Re-Verify Optical Signal Strength (Test Equipment)



Step 8. Begin Jitter Transfer Measurements.

8.3 How to measure Optical Intrinsic Jitter of the XRT91L80

To successfully perform this test, the user needs to configure the XRT91L80 into:

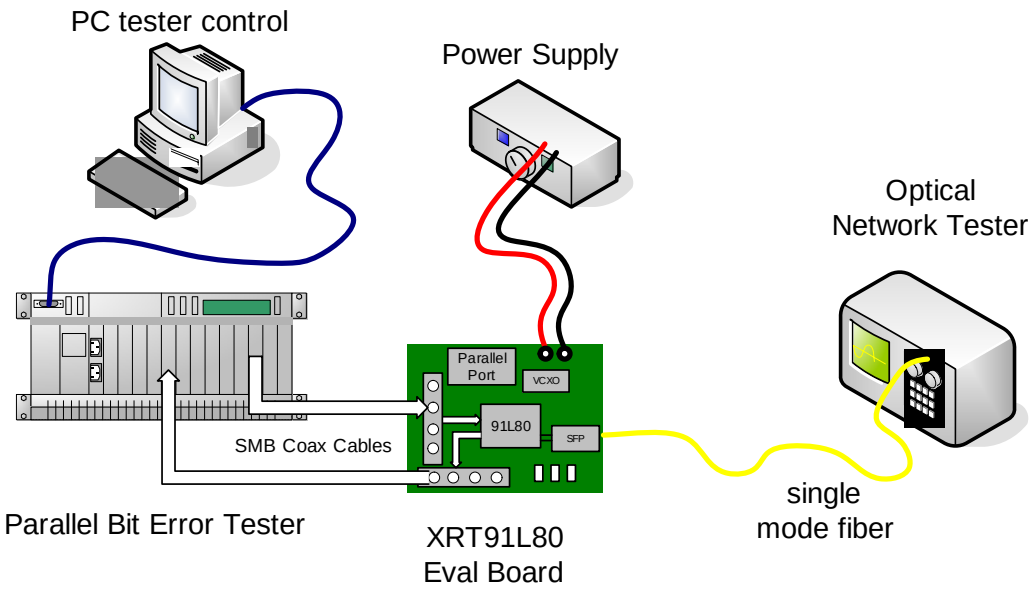
- Normal Mode (passing traffic in both directions)
- Local Timing Mode

In addition, the Parallel Bit Error tester must be configured to transmit:

- a fixed '1010' or '0101' pattern

Step 1. Set up the XRT91L80 Evaluation Board as outlined in section 4.2, "Setting up the XRT91L80 Evaluation Board for Parallel Bit Error Testing in Hardware Mode." Use high quality SMB coax cables to connect the Parallel Bit Error Tester to the XRT91L80 Evaluation Board. Once your setup is ready, follow the instructions on section 5.0, "Configuring the XRT91L80 for proper operation in Hardware Mode."

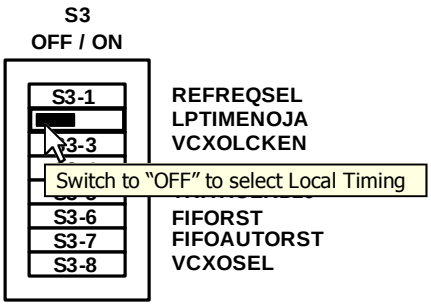
Figure 8.10 Intrinsic Jitter Measurement Test Setup



Step 2. Configure the Parallel Bit Error Tester to transmit a fixed '1010' or '0101' pattern.

Step 3. Select **Local Timing** mode for the XRT91L80 transmit timing.

Figure 8.11 Select Local Timing



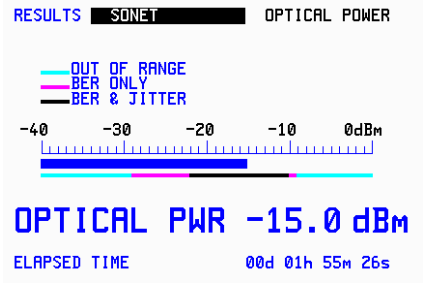
Step 4. Connect the optical cable from the OC-48/STM-16 SFP module to the Optical Network Test Equipment. Verify optical signal strength and attached an optical attenuator to the receiver end of the test equipment if necessary.

Step 5. Select the proper SONET/SDH data rate source on test equipment and verify test equipment is able to obtain valid signal from the XRT91L80 optical transmitter.

Note: Since the XRT91L80 is independently transmitting unframed '1010' or '0101' pattern from the Parallel Bit Error Tester to the SONET/SDH test equipment, data is not recovered by the SONET/SDH test equipment. Hence, data integrity and pattern sync on the tester is **not** expected. However, tester should detect an unframed OC48/STM-16 signal.

Step 6. Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler until desired optical signal strength is achieved for valid jitter measurements.

Figure 8.12 Verify Optical Signal Strength (Test Equipment)



Step 7. Configure the test equipment for jitter measurements and select the appropriate SONET STS-48/ SDH STM-16 jitter frequency filters on the test equipment according to the table below.

Table 2.0 SONET/SDH Jitter Frequency Bandpass Filters (1544 kb/s Networks)

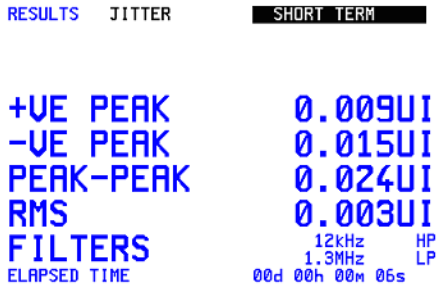
DATA RATE	SONET GR.253 FILTER STANDARD	SDH G.783 FILTER STANDARD
2488 Mbps	12 KHz – 20 MHz	12 KHz – 20 MHz

Table 2.1 SONET/SDH Jitter Frequency Bandpass Filters (2048 kb/s Networks)

DATA RATE	SONET GR.253 FILTER STANDARD	SDH G.783 FILTER STANDARD
2488 Mbps	12 KHz – 20 MHz	1 MHz – 20 MHz

Step 8. Begin measuring peak-to-peak jitter and permit test equipment to measure peak-to-peak and rms values over a sixty second interval per G.783 section 9.3.1.1.

Figure 8.13 RMS Jitter Measurement (Test Equipment)



9.0 XRT91L80 CURRENT CONSUMPTION MEASUREMENT

To successfully measure the current consumption on the XRT91L80, the user must have the following:

- A network test equipment capable of sourcing OC-48/STM-16.
- A current meter capable of measuring current accurately in milliamps.
- A volt meter capable of measuring voltage accurately in hundredths.
- The XRT91L80 Evaluation Board schematic for reference.

In addition, the user should configure the XRT91L80 to do the following:

- Remote Parallel Loopback
- Looptiming Mode

Step 1. Review the XRT91L80 Evaluation Board schematic and locate **L8, L9, L10, L11, L12, L13, L14, L15, L16, and L17**. These ferrite beads supply the entire power to the XRT91L80 silicon. Note that **L10, L11, L13, L14, L15, L16, and L17** ferrite beads lead to 1.8V power supply pins.

Step 2. Locate and remove the aforementioned ferrite beads on the XRT91L80 Evaluation Board. Store the ferrite beads in a secure container for reinstallation at a later time.

Step 3. Attach and secure jumper leads to **L8, L9, L10, L11, L12, L13, L14, L15, L16, and L17** soldering pads. These jumper leads should also be secured and prevented from physical stress when the current meter is attached to the leads. Check the soldering for shorts and remove errant solders on the board before proceeding. The board should be cleaned with a solder flux remover at the soldering site to prevent flux contamination and corrosion. Place all the jumpers on the jumper leads to close the circuit so that the XRT91L80 silicon can be powered.

Step 4. Adjust and verify 3.3V power supply with a Voltmeter. Connect 3.3V power supply to board using banana leads. Turn on power and verify power supply on the board by checking Power LED.

Step 5. Configure the XRT91L80 for Remote Parallel Loopback as outlined in section 6.1.2, “Remote Parallel Loopback.”

Step 6. Connect the optical cable from the OC-48/STM-16 SFP module to the Optical Network Test Equipment. Verify optical signal strength and attached an optical attenuator to the receiver end of the test equipment if necessary.

Step 7. Select the proper SONET/SDH data rate source and payload pattern on test equipment and verify recovered data integrity and pattern sync on test equipment. Do not forget to invoke a FIFO reset to clear the FIFO. Check test equipment for valid pattern synchronization.

Note: If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and verify data integrity. Check the jumper leads for proper solder and connection as well.

Step 8. Record the XRT91L80 current consumption and the voltage at each of the ferrite pad leads (**L8, L9, L10, L11, L12, L13, L14, L15, L16, and L17**) with reference to board Ground, the user will need this information to calculate the total power consumption. Note that Remote Parallel Loopback exercises all the logical blocks and analog drivers in the XRT91L80, thereby providing a worst case scenario for power consumption measurement.